Features

- **Specified Operating Voltage Range**
  Single supply voltage 4.5-5.5V
  Functions up to 7.0V
- **Specified Operating Temperature Range**
  From –40℃ up to 150℃
- **Linear Output with High Accuracy**
  12-bit Ratiometric Rail-to-rail output
  Digital Signal Processing
- **Magnetic Fields:**
  Static Fields and Dynamic Fields up to 2KHz
  Ranges between –100mT to +100mT
- **EEPROM Parameters Adjustment**
  Magnetic range and SNST
  Bandwidth setting
  Polarity of output curve
  Clamping option
  Temperature coefficient for all common magnets
  Memory Lock for Protection
- **Chip Protection:**
  Over Voltage and Under Voltage Detection
- **Supply Pulse Suppress Programming**
  2 wire programming interface
  Re-programmable until Memory Lock
  Individual Programming for Multiple Sensors
  Operation with the Same Supply and Ground
- **Calibration**
  2 Point Calibration
- **Industry standard SIP-4 Package, SOP-8 Package**

Applications

- Contactless Potentiometers
- Linear Position Sensing
- Angular Position Sensing
- Current Sensing
- Magnetic Field Measurement

General Description

MT1531 is a smart sensor providing an output voltage proportional to the magnetic flux through the hall plate and the supply voltage. It can be used for angle or distance measurements combined with a rotating or moving magnet.

MT1531 features a temperature-compensated Hall plate with chopper offset compensation, an A-to-D converter, digital signal processing, a D-to-A converter with output driver, an EEPROM memory with redundancy and lock function for the calibration data, a serial interface for programming the EEPROM, and protection devices at all pins.

MT1531 is fabricated in CMOS standard technology with embedded EEPROM and mixed-signal option devices.

Pin Configuration

Table 1-1：SIP-4 Pin Definition

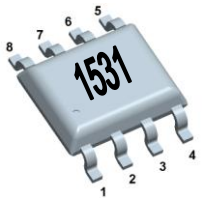
No	Pin	Function
1	VDD	Supply voltage / programming interface
2	GND	Ground
3	OUT	Output and selection pin
4	NC	No Connection

Figure 1-1: Pin definition on the SIP-4 package

Table 1-2: SOP-8 Pin Definition

No	Pin	Function
1	VDD	Supply voltage / programming interface
2	GND	Ground
3	OUT	Output and selection pin
4	NC	No Connection
5	NC	No Connection
6	NC	No Connection
7	NC	No Connection
8	NC	No Connection

Figure 1-2: Pin definition on the SOP-8 package



General

Transfer Function

Figure 2-1 shows one example of the chip operation.

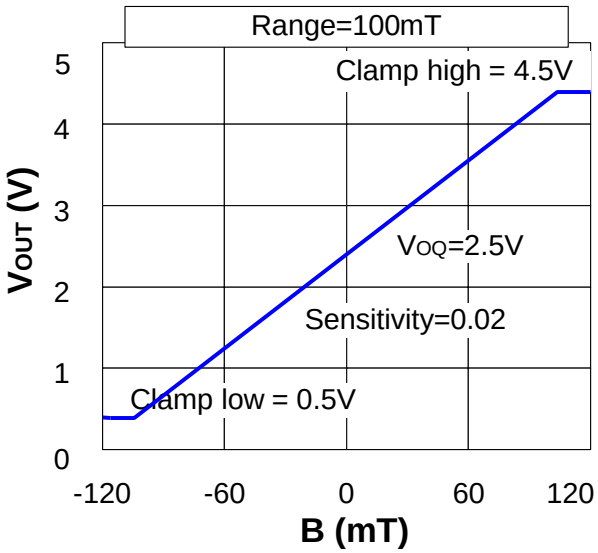


Figure 2-1: Example of Sensor Output

Block Diagram

Figure 2-2 shows the simplified block structure.

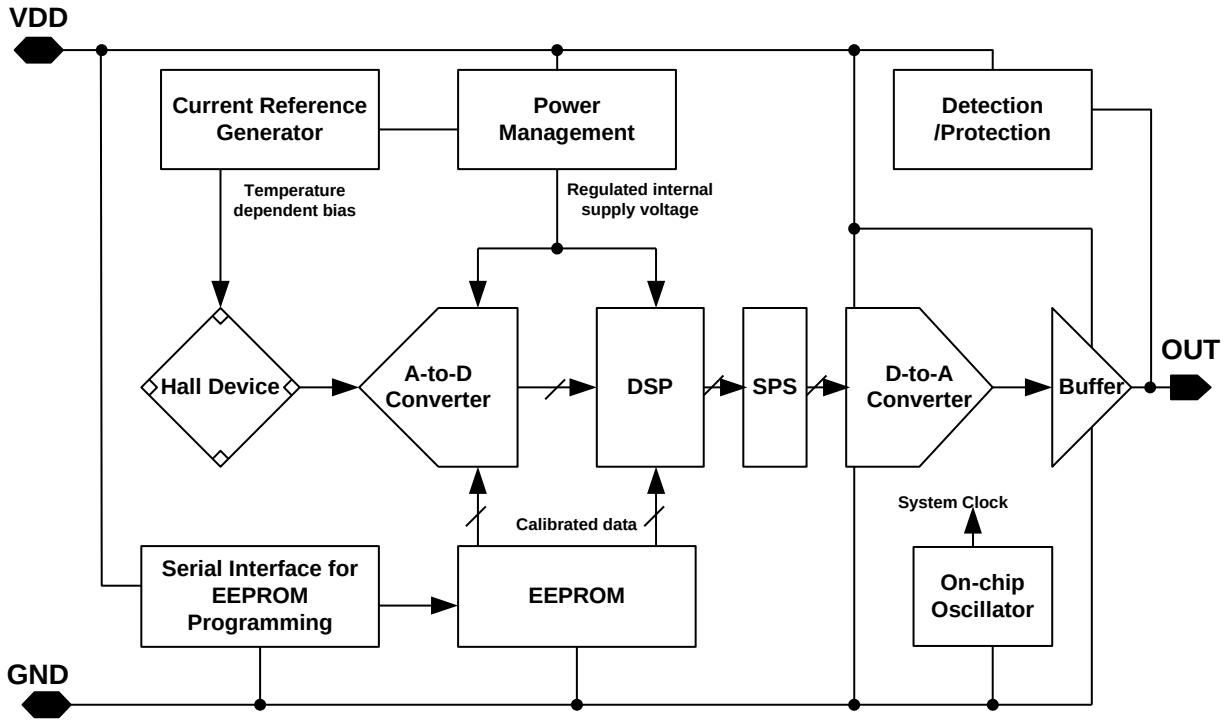


Figure 2-2: Block Diagram

Brief Theory of Operation

The magnetic flux is transferred to voltage signal by the Hall device
The output signal from the Hall device is converted to digital value through the ADC
Temperature compensation is processed by analog current bias
The output from ADC is processed by the DSP for range, gain and clamping, etc adjustment
The output from DSP is converted to analog value through the DAC
The output voltage is proportional to the supply voltage (ratiometric behavior)
Calibrate data is programmed to EEPROM by modulating the supply voltage

Register Functions

DSP and Registers

The DSP plays a major role in the signal conditioning. The parameters for the DSP are stored in the EEPROM registers, shown in Figure 3-1.

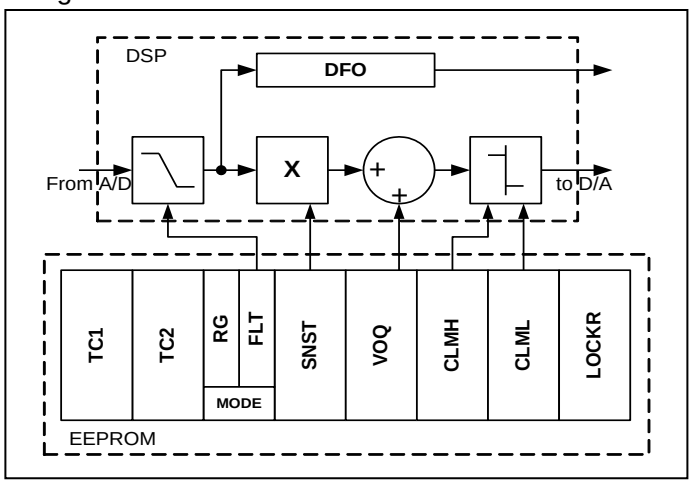


Figure 3-1: DSP and EEPROM customer registers

The EEPROM registers are divided into three groups.

Group 1 contains the registers for adjustment of the sensor to the magnetic system: MODE for selecting the magnetic field range and filter frequency, TC for the temperature characteristics of the magnetic sensitivity.

Group 2 contains the registers for the defining the output characteristics: SNST, VOQ, CLML, and CLMH. The output characteristic of the sensor is defined by these four parameters: (See Figure 2-1 as an example)

The parameter VOQ (Output Quiescent Voltage) corresponds to the output voltage at B=0.
The parameter Sensitivity defines the magnetic gain.

$$Sensitivity = \frac{\Delta Vout}{\Delta B}$$

The output voltage can be calculated as
VOUT ~ Sensitivity * B + VOQ

The output voltage range can be clamped by setting the registers CLML and CLMH in order to enable failure detection (such as short-circuits to VDD or GND and open connections).

An external magnetic field generates a Hall voltage on the Hall plate. The ADC converts the amplified positive or negative voltage (operates with magnetic north and south poles at the branded side of the package) to a digital value. Positive values correspond to a magnetic north pole on the branded side of the package. The digital signal is filtered in the internal low pass filter and is readable in DFO register. During further processing, the digital signal is multiplied with the sensitivity factor, added to the quiescent output voltage and limited according to the clamping voltage. The result is finally converted to an analog signal.

Register Description

MODE

Shown in Figure 3-2 Mode register is divided into 2 parts: Filter and Range.

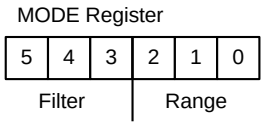


Figure 3-2: Mode register mapping

Range: The Range bits define the magnetic field range of the sensor.

Table 3-1: Setting of Range bits

Range	Magnetic Field Range
0	-100 mT ~ 100 mT
1	-30 mT ~ 30 mT
2	-60 mT ~ 60 mT
3	-80 mT ~ 80 mT

Filter: The Filter bits define the –3dB frequency of the digital low pass filter.

Table 3-2: Setting of Filter bits

Filter	-3dB Frequency
0	500 Hz
1	125 Hz
2	250 Hz
3	62.5 Hz
4	1 kHz
5, 6, 7	2 kHz

TC

The temperature dependence of the magnetic SNST can be adapted to different magnetic materials in order to compensate for the change of the magnetic strength with temperature. The adjustment is achieved by programming the TC (Temperature Coefficient) . The sensor can compensate for linear temperature coefficients ranging from –3100 ppm/K up to 400 ppm/K .

DFO

This 14-bit register delivers the actual digital value of the applied magnetic field before the signal processing. This register can be read out and is the basis for the calibration procedure of the sensor in the system environment.

The DFO at any given magnetic field depends on the programmed magnetic field range but also on the filter frequency.

Table 3-3: DFO range

Filter Frequency	DFO Effective Range
62.5 Hz	-32,768 ~ 32,767
125 Hz	-32,768 ~ 32,767
250 Hz	-32,768 ~ 32,767
500 Hz	-32,768 ~ 32,767
1 kHz	-32,768 ~ 32,767
2 kHz	-32,768 ~ 32,767

SNST

The SNST register contains the parameter for the multiplier in the DSP. The SNST is programmable between –4 and 4. For VDD=5V, the register can be changed in steps of 0.00012. SNST=1 corresponds to an increase of the output voltage by VDD if the DFO increases by 65536.

For calculations, the digital value from the magnetic field of the ADC converter is used. This digital information is readable from the DFO register.

$$Sensitivity = \frac{\Delta Vout * 65536}{\Delta DFO * VDD}$$

The register value is calculated by:

$$SNST = 8192 * Sensitivity$$

VOQ

The VOQ register contains the parameter for the adder in the DSP. VOQ is programmed from –2VDD up to 2VDD. For VDD=5V, the register can be changed in steps of 0.305mV.

The register value is calculated by:

$$VOQ = 16384 * \frac{V_{OQ}}{VDD}$$

For calibration in the system environment, a 2-point adjustment procedure is recommended. The suitable SNST and VOQ values for each sensor can be calculated individually by this procedure.

CLML and CLMH

The CLML register contains the parameter for the lower limit. The lower clamping voltage is programmable between 0 ~ VDD. For VDD=5V, the register can be changed in steps of 0.610mV

The CLMH register contains the parameter for the upper limit. The upper clamping voltage is programmable between 0 ~ VDD. For VDD=5V, the register can be changed in steps of 0.610mV
The register value is calculated by:

CLML=8192*(Low Clamping Voltage)/VDD
CLMH=8192*(High Clamping Voltage)/VDD

LOCKR

By setting this 8-bit register to 0B6H, all registers will be locked, and the sensor will no longer respond to any supply voltage modulation. This bit is active after the first power-off and power-on sequence after setting the LOCK byte.

Register List

Table 3-4: Customer register address

Register	Code	Bits	Format	Effective Range	Customer Operation	Notes
CLML	02~03H	13	Binary	0~8191	R/W/P	Low clamping voltage
CLMH	04~05H	13	Binary	0~8191	R/W/P	High clamping voltage
VOQ	06~07H	16	2's complement	-32768~32767	R/W/P	
SNST	08~09H	16	2's complement	-32768~32767	R/W/P	
MODE	0CH	6	Binary	0~63	R/W/P	Range and filter setting
LOCKR	01H	8	Binary	-	R/W/L	Lock bit
DFO	18~19H	16	2's complement	-32768~32767	R	
TC	0EH	8	Signed binary	-127~127	R/W/P	

Note:

1. R=READ, W=WRITE, P=Program, and L=LOCK
2. There are special bit reverse exist in CLMH and SNST:

CLMH: every bit is reversed. For example, writing 00011110101 is actually 11100001010 for real calculations.

SNST: only bit 13 is reversed. For example, writing 0000,0000,0000,0000 is actually 0000,0010,0000,0000 for real calculations (SNST=1).

VOQ: only bit 12 is reversed. For example, writing 0000,0000,0000,0000 is actually 0000,0010,0000,0000 for real calculations (VOQ=+0.5VDD)

Table 3-5: Reserved register address

Register	Code	Bits	Format	Range	Customer Operation	Notes
OFFS	0A~0BH	12	Binary	-2048~2047	-	
FOSCAD	17H	8	Binary	-128~127	-	
ID	00H	8	Binary	-	-	

Electrical and Magnetic Characteristics

Absolute Maximum Ratings

Absolute maximum ratings are limiting values to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.

Table 4-1: Absolute maximum ratings: all voltages listed are referenced to GND

Symbol	Parameters	Min	MAX	Unit	Notes
T_S	Storage temperature	-50	150	℃	
T_J	Junction temperature	-50	170	℃	
T_{SH}	Output short circuit duration		10	min	
VDD	Supply voltage	-1.0	13.8	V	t < 1min, $T_J < T_{JMAX}$
IDD_R	Reverse supply current		50	mA	$T_J \leq T_{JMAX}$
V_{OUT}	Output voltage	-5.0	13.8	V	t < 1min, $T_J < T_{JMAX}$
V_{OUT} - VDD	Output voltage over VDD		2	V	
I_{OUT}	Continuous output current	-10	10	mA	
Endurance	EEPROM programming cycles		200	Cycle	

Recommended Operating Conditions

Recommended operating conditions must not be exceeded in order to guarantee the performance of MT1531.

Table 4-2: Recommended operating conditions

Symbol	Parameters	Min	TYP	MAX	Unit	Notes
T_A	Ambient temperature	-40		150	℃	
T_J	Junction temperature	-40		170	℃	
VDD	Supply voltage	4.5	5.0	5.5	V	
I_{OUT}	Continuous output current	-1.0		1.0	mA	
C_L	Output load capacitance	0.33	10	1000	nF	

Electrical Characteristics

Table 4-3: Characteristics: at T_A=-40℃ to +150℃, VDD=4.5 to 5.5V, after programming and locking, at Recommend Operation Conditions if not otherwise specified. Typical values for T_A=25℃ and VDD=5V

Symbol	Parameters	Min	TYP	MAX	Unit	Conditions / Notes
I_{DD}	Supply current		7	10	mA	
V_{DDZ}	Over-voltage protection at VDD			14	V	I_{DD}=25mA, T_J=25C, 20ms
V_{OZ}	Over-voltage protection at Output			14	V	I_O=10mA, T_J=25C, 20ms
N_{RES}	Number of bit for resolution		12		Bit	Ratiometric to VDD
DNL	DAC differential non-linearity	-1		1	LSB	
INL	Output integrated non-linearity	-0.5		0.5	%	Percentage of VDD
E_R	Output ratiometric error in V_{OUT}/VDD	-0.5		0.5	%	$\lvert V_{OUT1}-V_{OUT2}\rvert$>2V during calibration *1
	Output ratiometricy $\frac{V_{OUT}(VDD)}{VDD} \Big/ \frac{V_{OUT}(VDD=5V)}{5V}$	99.5		100.5	%	$\lvert V_{OUT1}-V_{OUT2}\rvert$>2V during calibration
ΔT_K	Variation of linear temperature coefficient	-400		400	ppm/K	Suitable TC and TC2 for the application
ΔV_{OUTCL}	Accuracy of output voltage at clamping low voltage	-45		45	mV	RL=4.7kΩ, VDD=5V
ΔV_{OUTCH}	Accuracy of output voltage at clamping high voltage	-45		45	mV	RL=4.7kΩ, VDD=5V
V_{OUTCH}	Output high voltage	4.65	4.8		V	VDD=5V, $\lvert I_{OUT}\rvert$ <1mA
V_{OUTCL}	Output low voltage		0.2	0.35	V	VDD=5V, $\lvert I_{OUT}\rvert$ <1mA
F_{ADC}	ADC sampling frequency	-15%	320	+15%	kHz	
T_{RO}	Output response time		16 8 4 2 1.5 1	32 16 8 4 3 2	ms ms ms ms ms ms	F_{FILTER} = 62.5Hz F_{FILTER} = 125Hz F_{FILTER} = 250Hz F_{FILTER} = 500Hz F_{FILTER} = 1kHz F_{FILTER} = 2kHz CL=10nF, BINPUT is stepped from 0 to BMAX and 0% to 90% of output is measured
T_{DO}	Output delay time		0.1	0.5	ms	CL=10nF
T_{POD}	Output settling time during power up time		24 12 6	40 20 10	ms ms ms	F_{FILTER} = 62.5Hz F_{FILTER} = 125Hz F_{FILTER} = 250Hz

			3 2.5 2	5 4 3	ms ms ms	F_{FILTER} = 500Hz F_{FILTER} = 1kHz F_{FILTER} = 2kHz CL=10nF, settled to 90%
BW	Small signal bandwidth (-3dB)		2		kHz	B_{AC} < 10mT, F_{FILTER}=2kHz
V_{NOISE}	Output noise (peak-to-peak)		3	6	mV	Range=100mT, F_{FILTER}=62.5Hz SNST < 0.26 *2
R_{OUT}	Output resistance		1	10	ohm	V_{OUT} is in range
R_{thJA}	Thermal resistance junction to soldering point		150	200	K/W	

Note: 1. More than 50% of the selected magnetic field range is used and the temperature compensation is suitable.

2. Peak-to-peak value exceeded: 5%

Magnetic Characteristics

Table 4-4: Magnetic characteristics

Symbol	Parameters	Min	TYP	MAX	Unit	Conditions / Notes
B_{OFFSET}	Magnetic offset	-0.38	0	0.38	mT	B=0, I_{OUT}=0, T_J=25C
$\Delta B_{OFFSET}/\Delta T$	Magnetic offset versus T_J	-10	0	10	uT/K	B=0, I_{OUT}=0

4.5 Detection Parameters

Table 4-5: Detection parameters: at T_A=-40C to +150C

Symbol	Parameters	Min	TYP	MAX	Unit	Conditions / Notes
V_{OUTOD}	Output voltage at open VDD line	0		0.2	V	VDD=5V, RL=10kΩ
V_{OUTOG}	Output voltage at open GND line	4.7		5.0	V	VDD=5V, RL=10kΩ
VDD_{UV} *1	Under-voltage detection level	3.8		4.4	V	
VDD_{OV} *1	Over-voltage detection level	8.5		10.0	V	

Note: 1.Over-voltage and under-voltage detection is enabled only after locking.

Application Information

Application Schematics

Figure 5-1 shows a typical application schematic using a single MT1531 sensor. Two capacitors are recommended to connect between VDD to GND and OUT to GND respectively, to improve EMC.
Resistive load no less than 4.7kΩ is permitted at OUTPUT.

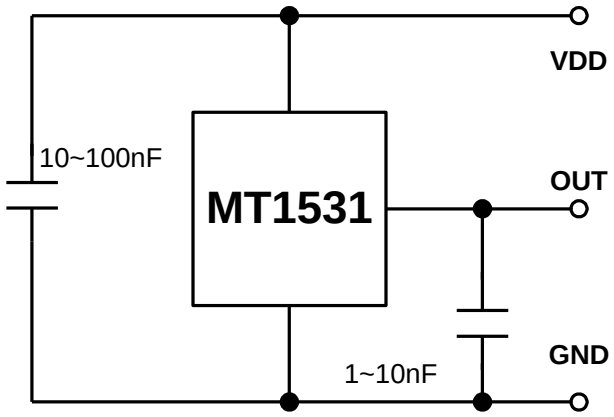


Figure 5-1: Recommended circuit for MT1531

Calibration

Recommended two-point adjustment for calibration is discussed.

Step 1: Input of the registers for general setting
The magnetic circuit, the magnetic material with its temperature characteristics, the filter frequency, and low and high clamping voltage are given for this application.

Therefore, the values of the following registers should be identical for all sensors of the customer application.

FILTER
According to the maximum signal frequency
RANGE
According to the maximum magnetic field at the sensor position
TC
Depends on the material of the magnet and the other temperature dependencies of the application
CLML and CLMH
According to the application requirements
Write the appropriate settings into the registers.

Step 2 Calculations of VOQ and SNST

The calculation points 1 and 2 can be set inside the specified range. The corresponding values for VOUT1 and VOUT2 result from the application requirements.

Low clamping voltage ≤ VOUT1,2 ≤ High clamping voltage

For highest accuracy of the sensor, calibration points near the minimum and maximum input signal are recommended. The difference of the output voltage between calibration point 1 and calibration point 2 should be more than 2.5V.

Set the system to calibration point 1 and read the register DFO. The result is the value DFO1.

Now, set the system to calibration point 2, read the register DFO again, and get the value DFO2.

With these values and the target values VOUT1 and VOUT2, for the calibration points 1 and 2, respectively, the values for SNST and VOQ are calculated as:

$$Sensitivity = \frac{V_{OUT1} - V_{OUT2}}{DFO1 - DFO2} \cdot \frac{65536}{VDD}$$

$$V_{OQ} = V_{OUT1} - \frac{DFO1 \cdot Sensitivity \cdot VDD}{65536}$$

This calculation has to be done individually for each sensor.

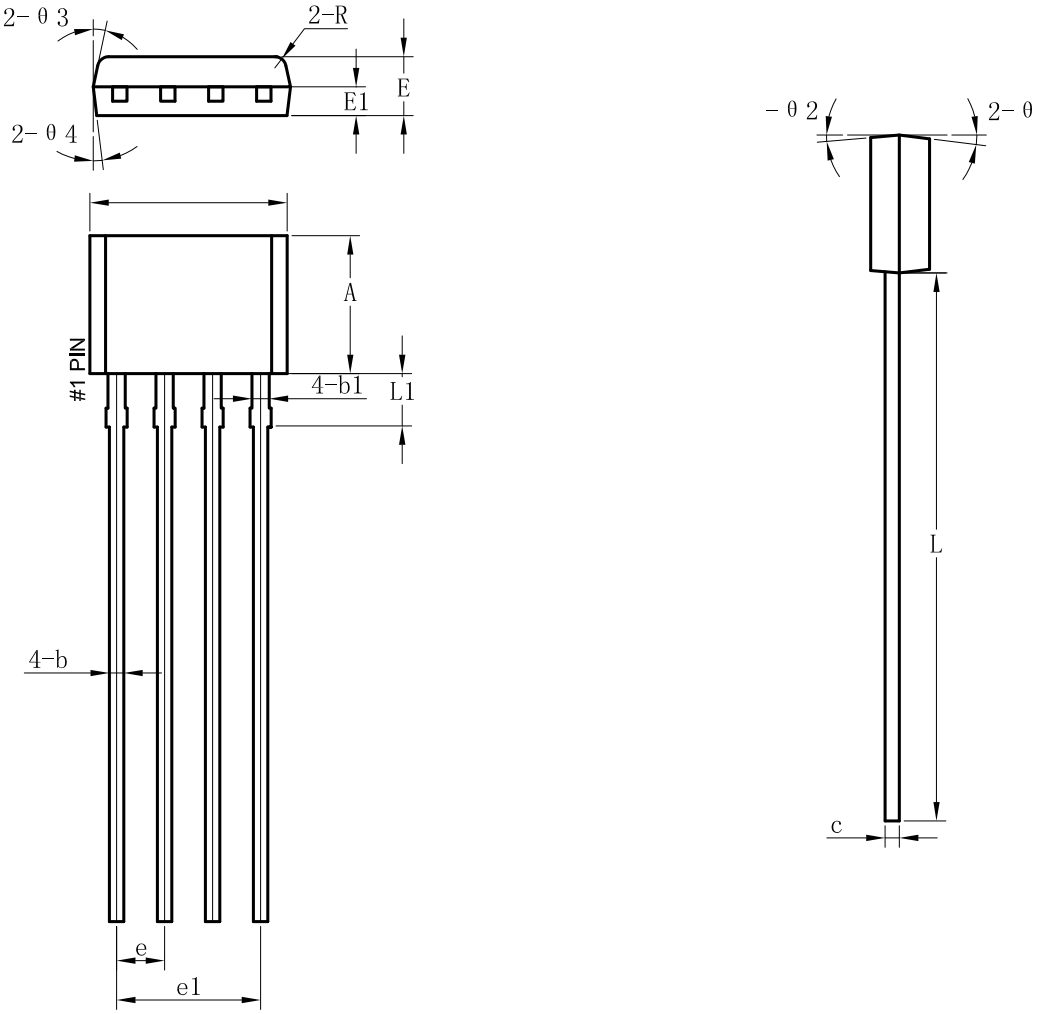
Next, write the calculated values for SNST and VOQ into the chip for adjusting the sensor.

Step 3 Locking the Sensor

The last step is activating the LOCK function with the “LOCK” command. Please note that the LOCK function becomes effective after power-down and power-up of the Hall IC. The sensor is now locked and does not respond to any programming or reading commands.

PACKAGE DESIGNATOR

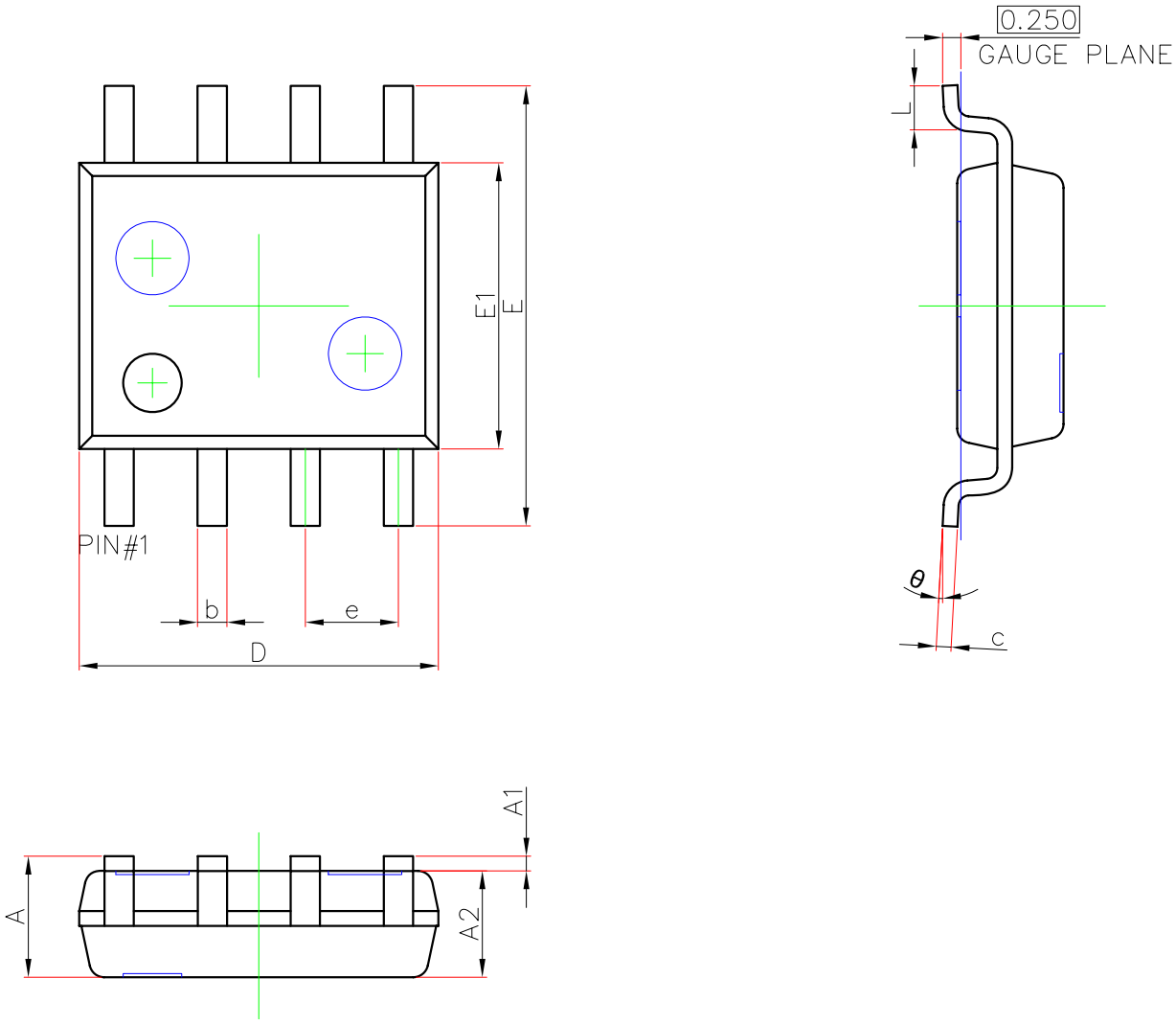
1531 Flat TO-94



Symbol	Dimensions in Millimeters		
	Min	Typ	Max
A	3.55	3.65	3.75
b	0.35	0.39	0.56
b1	-	0.46	-
c	0.36	0.38	0.51
D	5.12	5.22	5.32
E	1.46	1.56	1.66
E1	-	0.76	-
e	-	1.27	-
e1	-	3.81	-
L	13.5	14.5	15.5
L1	-	1.42	-
R	-	0.3	-
θ 1	-	6°	-
θ 2	-	4°	-
θ 3	-	11°	-
θ 4	-	6°	-

PACKAGE DESIGNATOR

(MT1531CT) SOP-8



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
e	1.270(BSC)		0.050(BSC)	
L	0.400	0.800	0.016	0.031
θ	0°	8°	0°	8°