Features and Benefits

- Based on advanced magnetic field sensing technology
- Non-contacting angle measurement and large air gap
- Up to 15krpm with propagation delay compensation
- Independent output interfaces: I^2C, SPI, Analog and PWM
- 14bit core resolution
- User programmable resolution & zero index position
- RoHS Compliant 2011/65/EU
- SOP-8 or QFN-16 Package

Applications

- Replacement of optical encoders
- Robotics control
- BLDC motor commutation
- Power tools

1. General Description

The MagnTek rotary position sensor MT6813 is based on advanced magnetic field sensing technology. The sensor contains two magnet field sensing element arrays. A rotating magnetic field in the x-y sensor plane delivers two sinusoidal output signals indicating the angle (α) between the sensor and the magnetic field direction. Within a homogeneous field in the X-Y plane, the output signals are relatively independent of the physical placement in the z direction.

The sensor is only sensitive to the magnetic field direction as the sensing element output is specially designed to be independent from the magnet field strength. This allows the device to be less sensitive to magnet variations, stray magnetic fields, air gap changes and off-axis misalignment.

A standard I^2C or SPI (3-wire or 4-wire) interface allows a host microcontroller to read 14-bit absolute angle position data from MT6813.

The absolute angle position is also provided as PWM output or an analog signal proportional to VDD from a 12bit DAC.

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2. Pin Configuration

2.1. SOP-8 Package

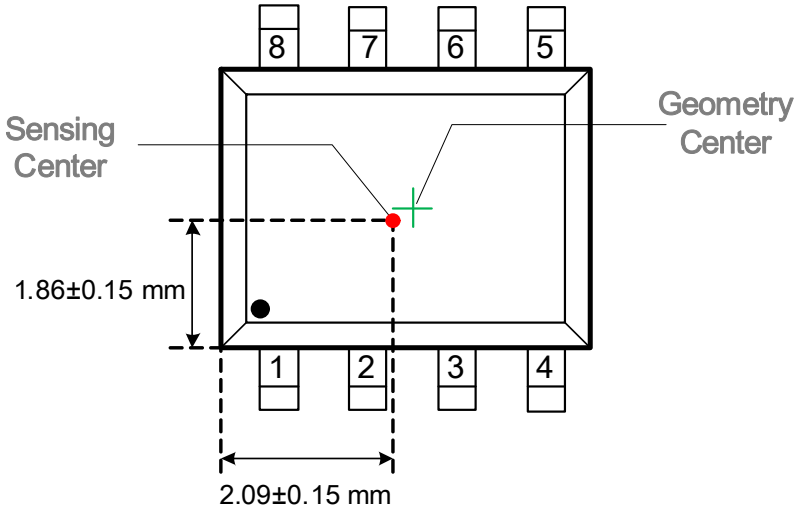


Figure 1: Pin Configuration for SOP-8 Package

Pin Name	#	Type	Description
CSN	1	Digital Input	I^2C/SPI Selection
HVPP	2	Analog Input	OTP Programming Supply or SPI/I^2C Selection
OUT	3	Analog/Digital Output	Analog or PWM Output
VDD	4	Power Supply	3.3~5.0V Supply
MOSI/SDAT/SDA	5	Digital Input/Output	SPI MOSI, SDAT or I^2C Data
MISO	6	Digital Input/Output	SPI MISO
SCK/SCL	7	Digital Input/Output	SPI clock or I^2C Clock
GND	8	Ground	Ground

Family Members

Part number	Description
MT6813CT	SOP-8 package, tube pack (100pcs/tube) or tape & reel pack (3000pcs/reel)

SOP-8 Reflow Sensitivity Classification: MSL 3

2.2. QFN-16 Package

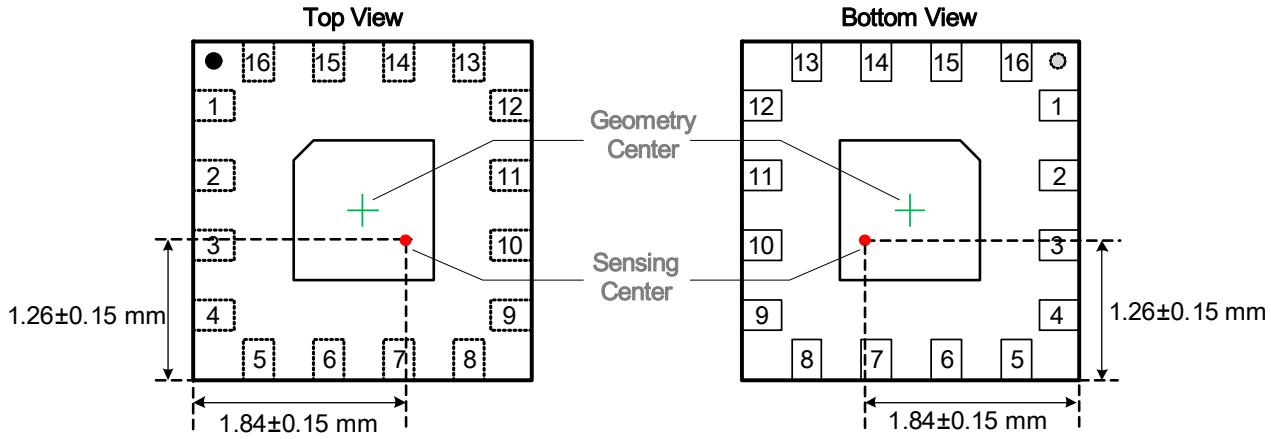


Figure 2: Pin Configuration for QFN-16 Package

Pin Name	#	Type	Description
MOSI/SDA	1	Digital Input/Output	SPI MOSI or I^2C Data
MISO	2	Digital Input/Output	SPI MISO
SCK/SCL	3	Digital Input/Output	SPI clock or I^2C Clock
GND	4	Ground	Ground
CSN	5	Digital Input	SPI/I^2C Selection
NC	6	NC	NC
NC	7	NC	NC
NC	8	NC	NC
NC	9	NC	NC
NC	10	NC	NC
OUT	11	Analog/Digital Output	Analog or PWM Output
HVPP	12	Analog Input	OTP Programming Supply or SPI/I^2C Selection
NC	13	NC	NC
NC	14	NC	NC
NC	15	NC	NC
VDD	16	Supply	3.3~5.0V Supply

Family Members

Part number	Description
MT6813QT	QFN-16 package, tape and reel pack (3000pcs/reel)

QFN-16 Reflow Sensitivity Classification: MSL 3

3. Functional Diagram

The MT6813 is manufactured in a CMOS standard process and uses advanced magnet sensing technology to sense the magnetic field distribution across the surface of the chip. The integrated magnetic sensing element array is placed around the center of the device and delivers a voltage representation of the magnetic field at the surface of the IC.

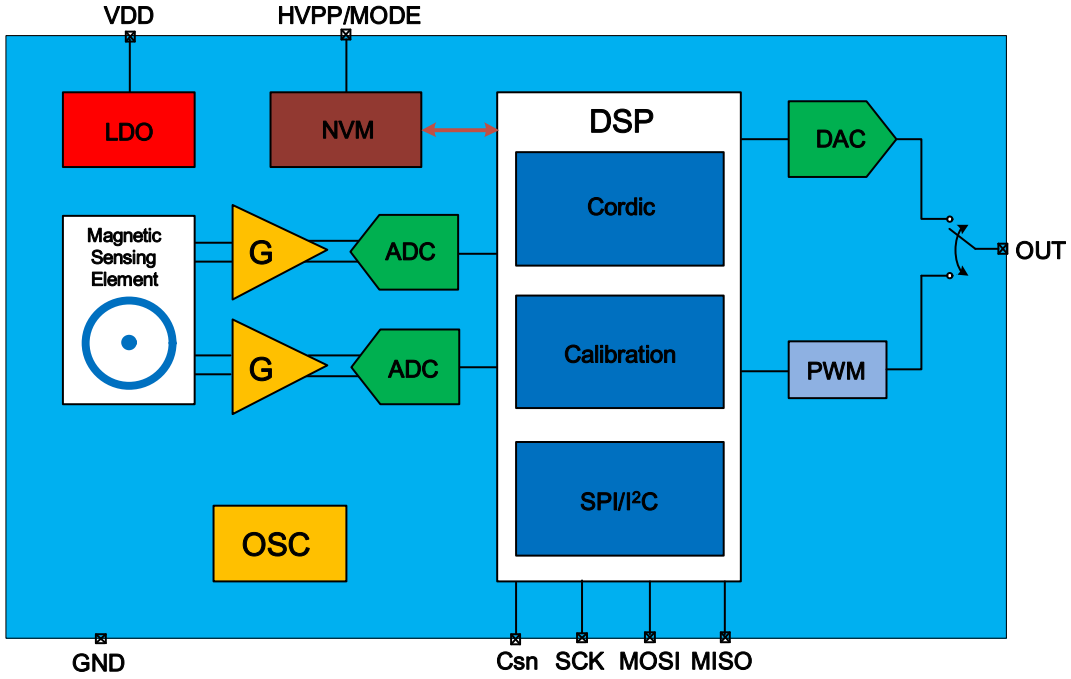


Figure 3: Simplified System Block Diagram

Figure 3 shows a simplified block diagram of the chip, consisting of the magnetic sensing element modeled by two interleaved Wheatstone bridges to generate cosine and sine signals, gain stages, analog-to-digital converters (ADC) for signal conditioning, and a digital signal processing (DSP) unit for encoding. Other supporting blocks such as LDO, etc. are also included.

4. Absolute Maximum Ratings (Non-Operating)

Stresses beyond those listed under “Absolute Maximum Ratings “may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under “Operating Conditions” is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameter	Notes	Min.	Max.	Unit
DC voltage at pin VDD	-	-0.5	7	V
DC voltage at pin HVPP	-	-0.5	8	V
Storage temperature	-	-55	150	°C
Operating Temperature	-	-40	125	°C
Electrostatic discharge (HBM)		± 3		kV
Electrostatic discharge (CDM)		± 1.5		kV

5. Electrical Characteristics

Operating conditions: Ta= -40 to +150°C, VDD= 3.0-5.5V unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
VDD	Supply Voltage	-	3.0	3.3~5.0	5.5	V
HVPP	Supply Voltage	-	6.75	7.0	7.25	V
Idd	Supply Current	-	-	6.0	9.0	mA
INL	Integral Non-Linearity	Note (1)	-	±1	±1.5	Degrees
T_{PwrUp}	Power-up Time	VDD Ramp<10us	-	-	1.0	ms
Analog Output Characteristics						
R_{OUT}	Analog Output Resistance	-		15	30	Ω
R_L	Pull-Up or Pull-Down	-	1K	-	-	Ω
C_L	Loading Capacitor	-	-	-	100	nf
V_{Sat_High}	Saturation High Voltage	I_{Load}=1mA	95	98		%VDD
V_{Sat_Low}	Saturation Low Voltage	I_{Load}=1mA		2	5	%VDD
DAC_LSB	DAC LSB	12-bit DAC		0.025		%VDD
DAC_INL	DAC Integral Non-Linearity				±3	LSB
DAC_DNL	DAC Differential Non-Linearity				±1.5	LSB
V_{Noise}	Analog Output Noise	Ta=25°C, RMS value, excluding DAC quantization noise			0.02	%VDD
Erm	Ratiometric Error	Note (2)	-0.3		0.3	%
PWM Output Characteristics						
FPWM	PWM Frequency	Programmable	625		5000	Hz
T_{Rise}	Rising Time	C_{Load}=1nf			1	us
T_{Fall}	Falling Time	C_{Load}=1nf			1	us
Digital I/O Characteristics (Push-Pull Type in Normal Mode)						
V_{IH}	High level input voltage	-	0.7*VDD	-	-	V
V_{IL}	Low level input voltage	-	-	-	0.3*VDD	V
V_{OH}	High level output voltage	I_{OH}=2mA	VDD-0.1	-		V
V_{OL}	Low level output voltage	I_{OL}=2mA	-	-	0.1	V
I_{LK}	Input Leakage Current	-	-	-	±1	μA

Note (1): The typical error value can be achieved at room temperature and with no off-axis misalignment error. The max error value can be achieved over operation temperature range, at maximum air gap and with worst-case off-axis misalignment error.

Note (2): The analog output is by design ratiometric, i.e. it is proportional to the supply voltage VDD. The ratiometric error is calculated as follows.

$$\text{Erm} = [\frac{Vout(V_{DD})}{V_{DD}} - \frac{Vout(5\text{V})}{5V}] \cdot 100\%$$

6. Magnetic Input Specification

Operating conditions: Ta= -40 to +125°C, VDD= 3.0-5.5V unless otherwise noted. Two-pole cylindrical diametrically magnetized source.

Symbol	Parameter	Notes	Min	Typ	Max	Unit
Dmag	Diameter	Recommended magnet: Ø8mm x 2.5mm for cylindrical magnets		8	-	mm
Tmag	Thickness	-		2.5	-	mm
Bpk	Magnetic input field amplitude	Measured at the IC surface.	200	-	10000	Gauss
AG	Air Gap	Magnet to IC surface distance (Figure 4)		-	3.0	mm
RS	Rotation Speed		-	- -	15	KRPM
DISP	Off Axis Misalignment	Misalignment error between sensor center and magnet axis (Figure 4)	-	-	0.3	mm
TCmag1	Recommended magnet material and temperature drift	NdFeB (Neodymium Iron Boron)	-	-0.12	-	%/°C
TCmag2		SmCo (Samarium Cobalt)	-	-0.035	-	

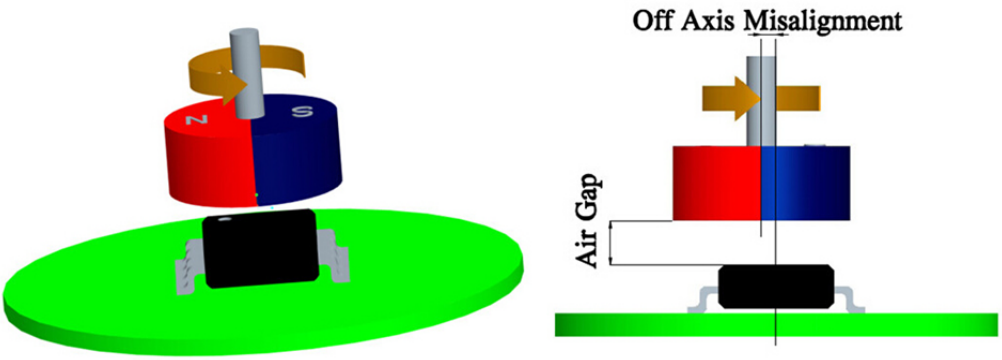


Figure 4: Magnet Arrangement

7. Output Mode

The MT6813 provides Analog and PWM output modes. Also angle data could be transferred by I^2C or SPI interface.

7.1. I/O Pin Configuration

For SOP-8 Package, I^2C and SPI are configured to Pin.5, Pin.6, and Pin.7. Analog or PWM output is configured to Pin.3.

SOP-8 Package I/O Pin configuration:

Mode / Pin #	I^2C	3 Wire SPI	4 Wire SPI
5	SDA	SDAT	MOSI
6			MISO
7	SCL	SCK	SCK

For QFN-16 Package, I^2C and SPI are configured to Pin.1, Pin.2 and Pin.3. Analog or PWM output is configured to Pin.11.

QFN-16 Package I/O Pin configuration:

Mode / Pin #	I2C	3 Wire SPI	4 Wire SPI
1	SDA	SDAT	MOSI
2			MISO
3	SCL	SCK	SCK

7.2. Analog Output Mode

The MT6813 provides a rail-to-rail linear analog output by a build-in 12 bit DAC as shown in Figure 5. It's a linear transfer function of absolute angle and output voltage. To enable analog output, register 'Enable Analog' should be programmed to high.

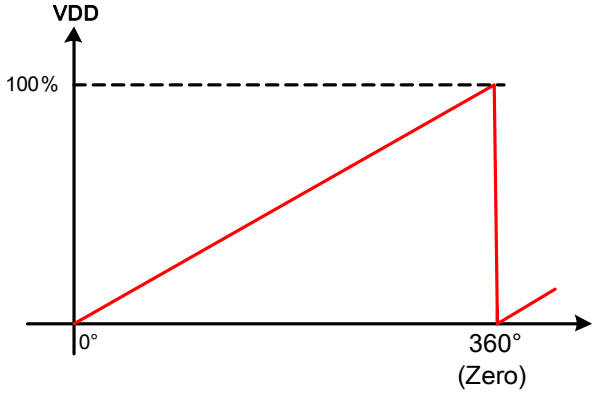


Figure 5: Default Analog Output

Analog or PWM Output Control Register (OTP)

Reg. Enable Analog	Pin.3(SOP-8), Pin.11(QFN-16)
0	PWM
1	Analog

The reference circuit for analog output is shown in Figure 6, an external decoupling capacitor C1 (typical 10nf, maximum 100nf) is suggested for better performance.

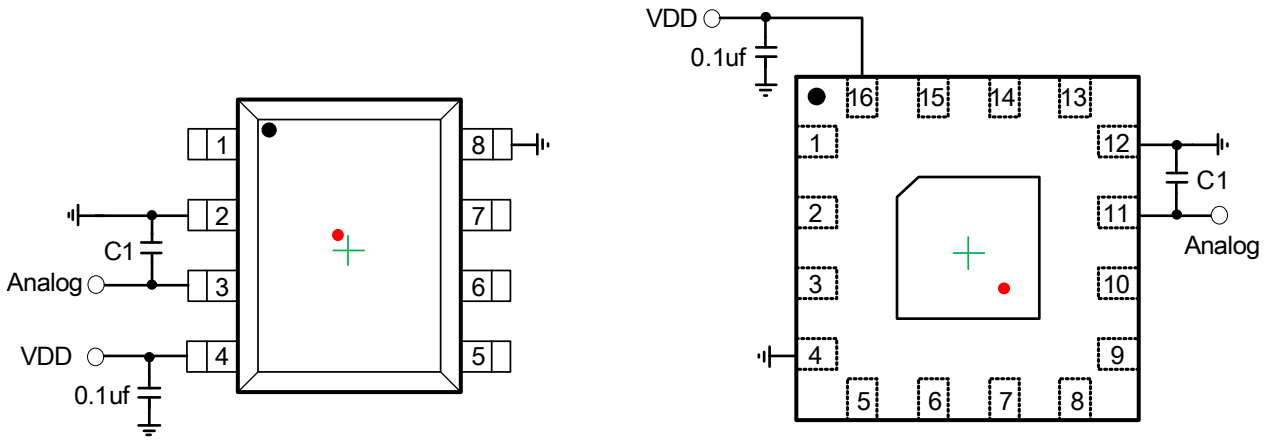


Figure 6: Analog Output Reference Circuit

The angle and voltage value of start-point, stop-point, Clamp_Low and Clamp_High could be programmed, also a Zero point could be programmed as shown in Figure 7.

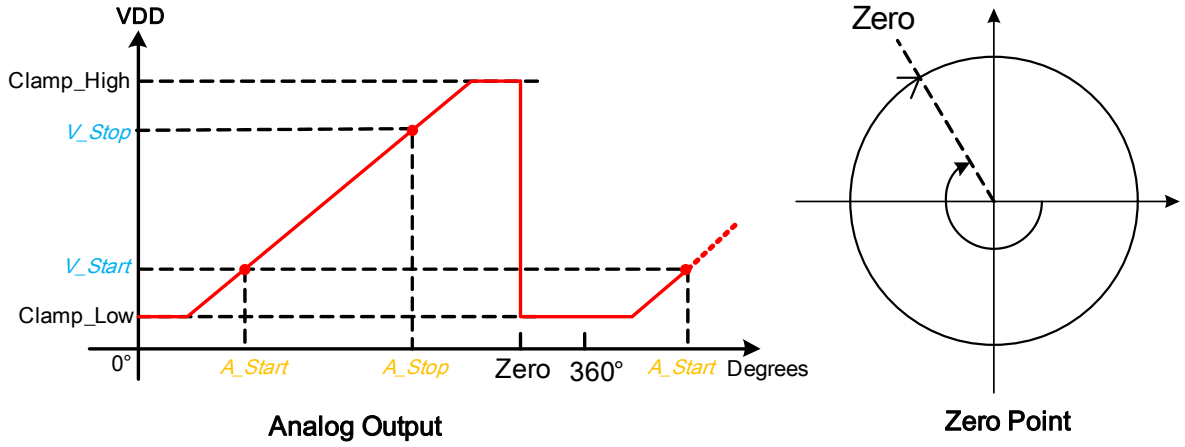


Figure 7: Analog Output Transfer function and Zero Point

Analog Output Registers (MTP)

Reg.	Bit<7:4>	Bit<3:0>
Clamp_Low_LSB	Clamp_Low<7:0>	
Clamp_High_LSB	Clamp_High<7:0>	
Clamp_Msb	Clamp_High<11:8>	Clamp_Low<11:8>
Zero_Lsb	Zero<7:0>	
Zero_Msb	NA	Zero<11:8>
Start_Anlge_Lsb	A_Start<7:0>	
Start_Angle_Msb	NA	A_Start<11:8>
Stop_Angle_Lsb	A_Stop<7:0>	
Stop_Angle_Msb	NA	A_Stop<11:8>
Start_Voltage_Lsb	V_Start<7:0>	
Stop_Voltage_Lsb	V_Stop<7:0>	
Voltage_Msb	V_Stop<11:8>	V_Start<11:8>

7.3. Pulse Width Modulation (PWM) Output Mode

The MT6813 provides a digital Pulse Width Modulation (PWM) output, whose duty cycle is proportional to the measured angle as shown in Figure 9. PWM is a default output of Pin.3 (SOP-8) and Pin.11 (QFN-16).

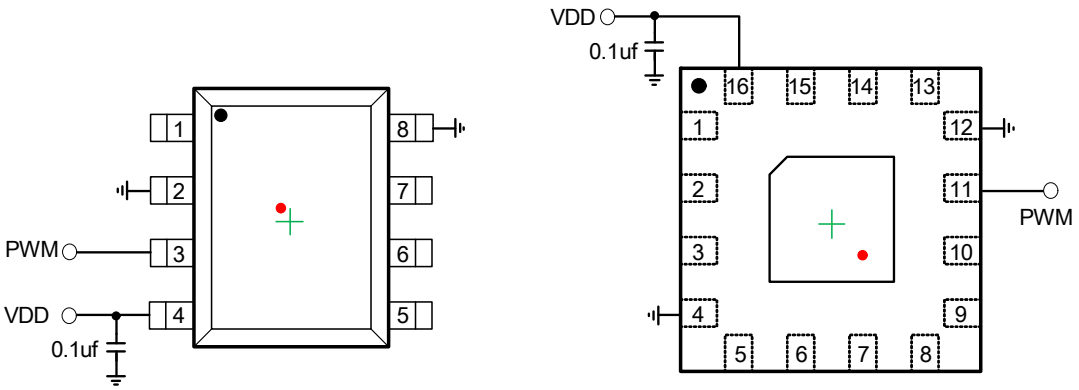


Figure 8: PWM Output Reference Circuit

PWM Resolution Register (OTP)

Reg. PWM_Res<1:0>	Resolution	PWM Frequency
00	10 bit	2.5 KHz
01	9 bit	5 KHz
10	11 bit	1.25 KHz
11	12 bit	625 Hz

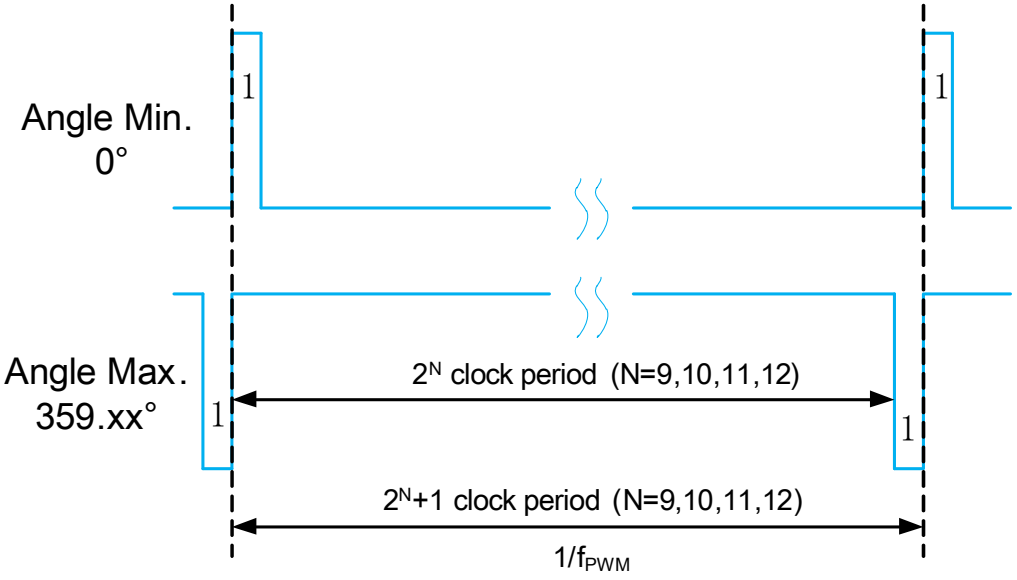


Figure 9: PWM Output

7.4. I²C Interface

The MT6813 provide a slave I²C interface for host MCU to read back digital absolute angle information from its internal registers. The reference circuit for I²C interface is shown in Fig 10, whether the need for pull-up resistor on SCL is determined by MCU, for MT6813 SCL is a digital input.

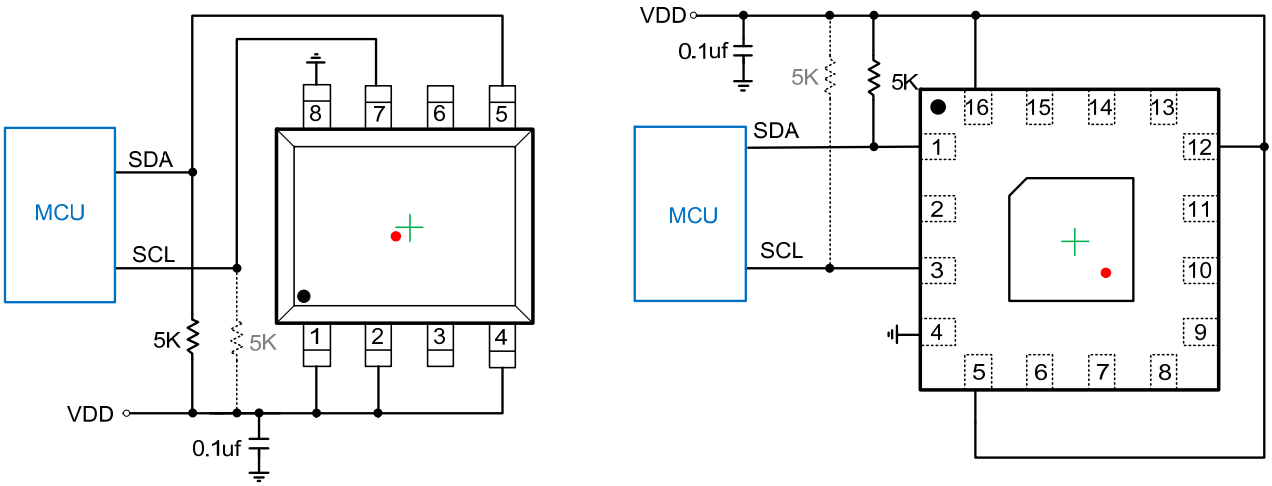


Figure 10: I²C Reference Circuit

7.4.1. I²C Timing Diagram

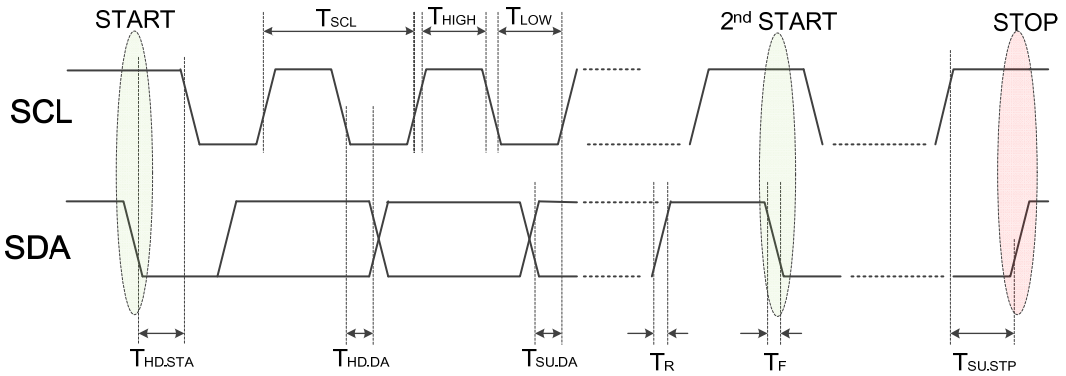


Figure 11: I²C Timing Diagram

I²C Timing Parameter

Symbol	Notes	Min	Max.	Unit
T_{SCL}	SCL clock period	1		μs
$T_{HD.STA}$	Hold Time of 'START'	250		ns
T_{LOW}	Low phase of SCL	250		ns
T_{HIGH}	High phase of SCL	250		ns
$T_{SU.DA}$	Setup Time of SDA	100		ns
$T_{HD.DA}$	Hold Time of SDA	50		ns
T_R	Rising Time of SDA/SCL		150	ns
T_F	Falling Time of SDA/SCL		150	ns
$T_{SU.STP}$	Setup Time of 'STOP'	250		ns

7.4.2. I²C Read Angle Registers

The slave ID of MT6813 is b'0000110 in 7 bit binary form. The 14 bits angle data is stored in internal register 0x03 and 0x04. Please follow the I²C timing of Figure 12 to read the angle data from 0x03 and 0x04.

Note: Please read register 0x03 first and then read 0x04

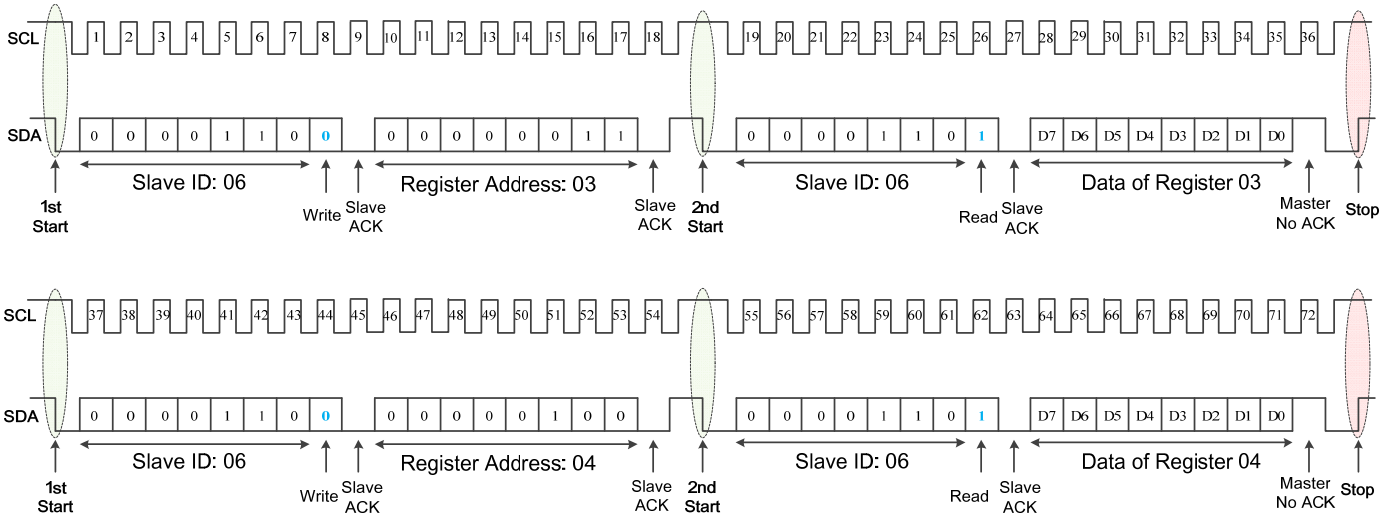


Figure 12: I²C Single Byte Read

Angle Data Register

Reg. Addr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0X03	Angle<13:6>							
0X04	Angle<5:0>						No_Mag_Warning	Parity Check

0~360° absolute angle θ could be calculated by the below formula:

$$\theta = \frac{\sum_{i=0}^{13} 2^{Angle<i>}}{8192} \bullet 360°$$

Parity Check

Bit 0x04[1] is a diagnosed bit for No Magnet Detected. When the MT6813 could not detect enough magnetic field for proper operation, this bit is set to high.

Bit 0x04[0] is a parity check bit for the data of 0x03[7:0] and 0x04[7:1]. When the 15 bits of 0x03[7:0] and 0x04[7:1] have an odd number of logic '1', 0x04[0]=1, otherwise 0x04[0]=0.

e.g. Under normal operation, get data 0x03=8F, 0x04=19, the parity check is correct
e.g. Under normal operation, get data 0x03=8F, 0x04=18, the parity check is wrong.

7.4.3. I²C Burst Read

The MT6813 provides an I²C burst read mode as shown in Figure 13 for faster data rate than single byte read mode.

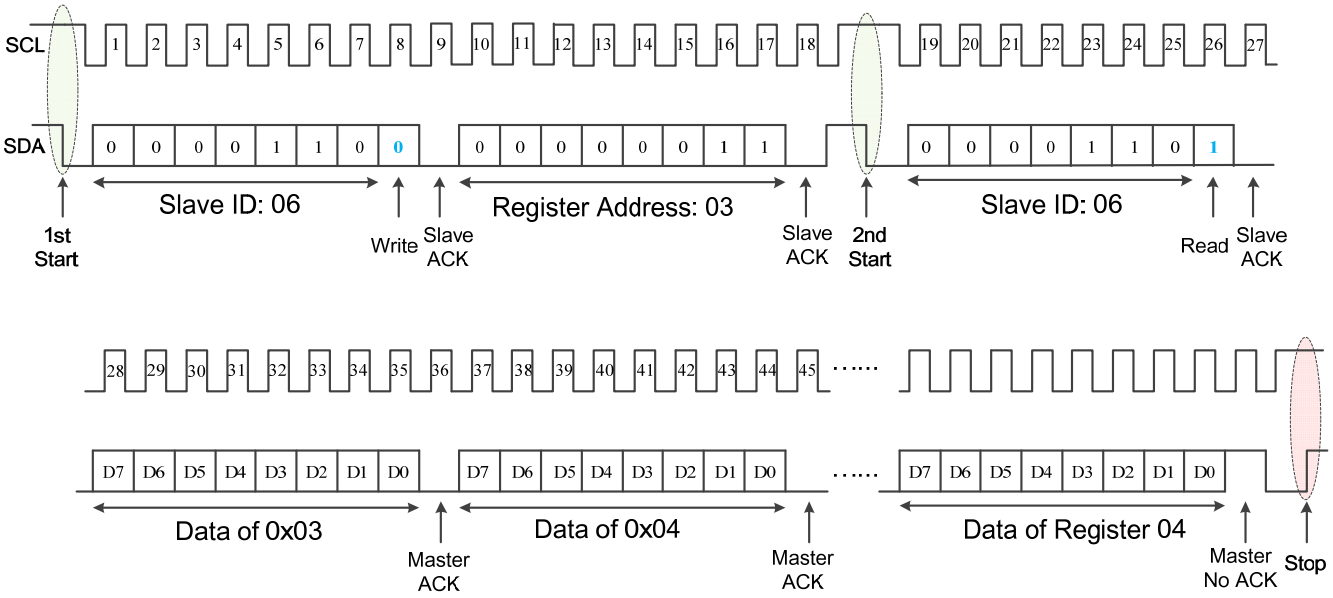


Figure 13: I²C Burst Read

7.4.4. I²C Write

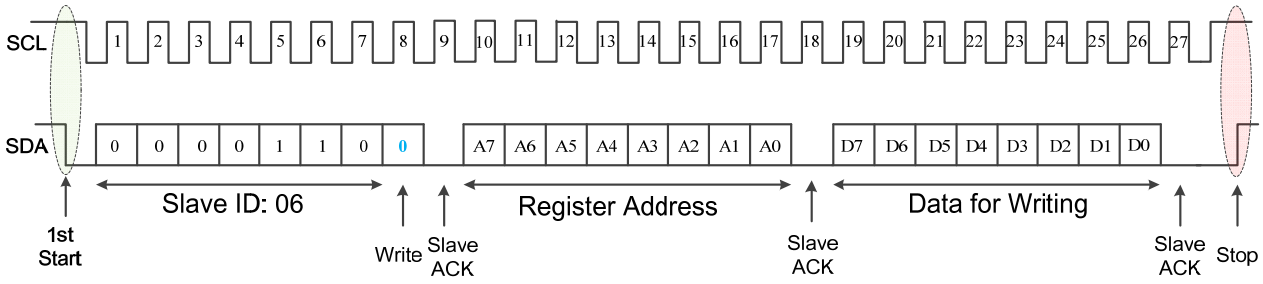


Figure 14: I²C Write

7.5. SPI Interface

The MT6813 also provides a 4-Wire or 3-Wire SPI (Register 3W_SPI should be programmed t to 'High' to enable 3-Wire SPI Mode) interface for host MCU to read back digital absolute angle information from its internal registers. The reference circuit for SPI interface is shown in Figure 15 and Figure 16.

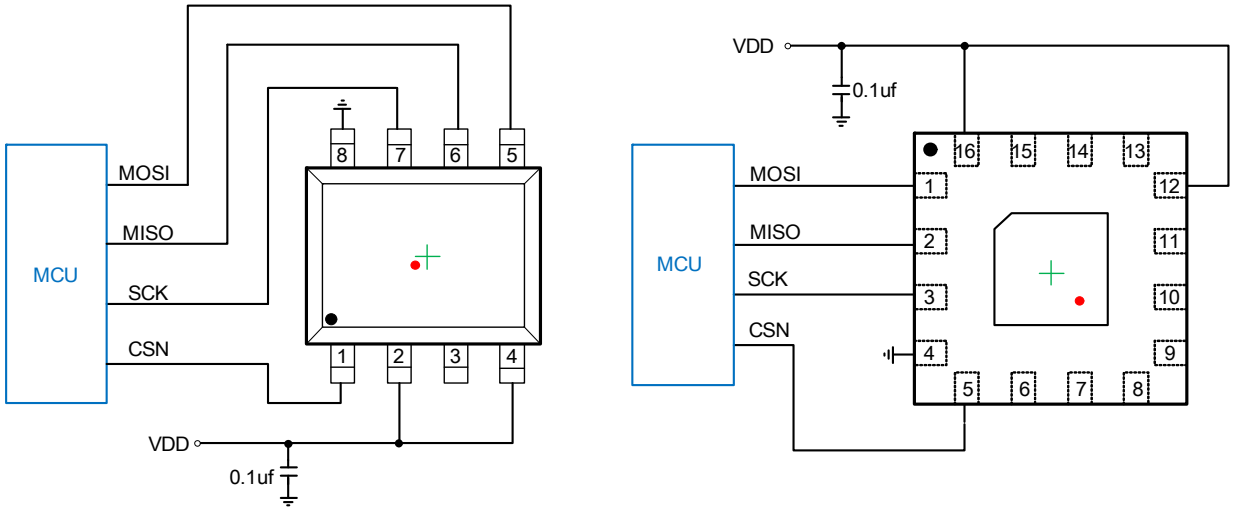


Figure 15: 4-Wire SPI Reference Circuit

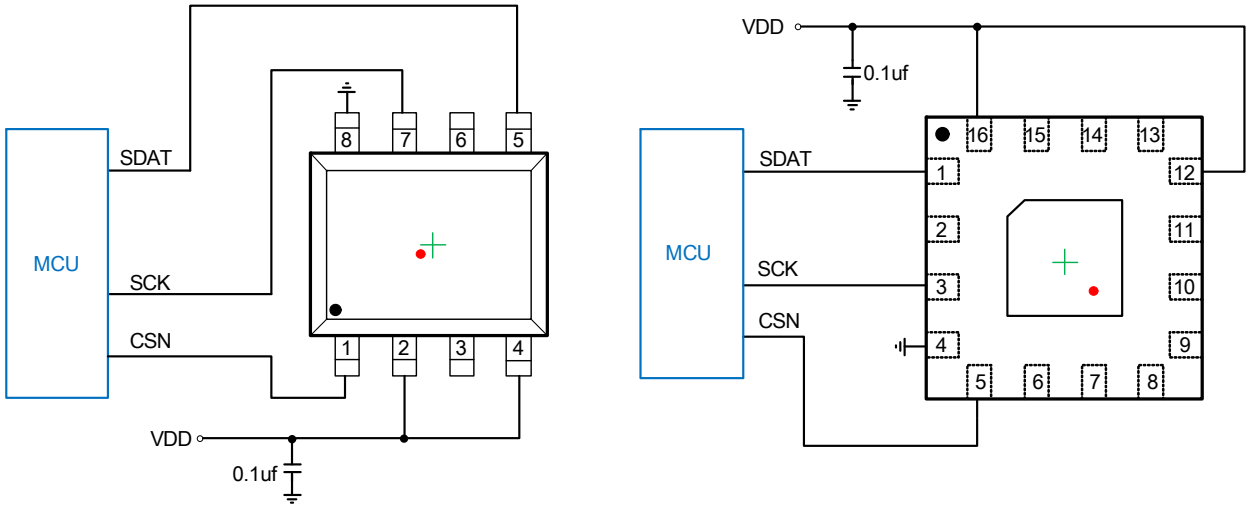


Figure 16: 3-Wire SPI Reference Circuit

3-Wire SPI Enable Register (OTP)

Reg. 3W_SPI	SPI Interface
0	4 Wire
1	3 Wire

7.5.1. SPI Timing Diagram

The MT6813 SPI uses mode=3 (CPOL=1, CPHA=1) to exchange data. As shown in Figure 17, a data transfer starts with the falling edge of CSN. The MT6813 samples data on the rising edge of SCK, and the data transfer finally stops with the rising edge of CSN.

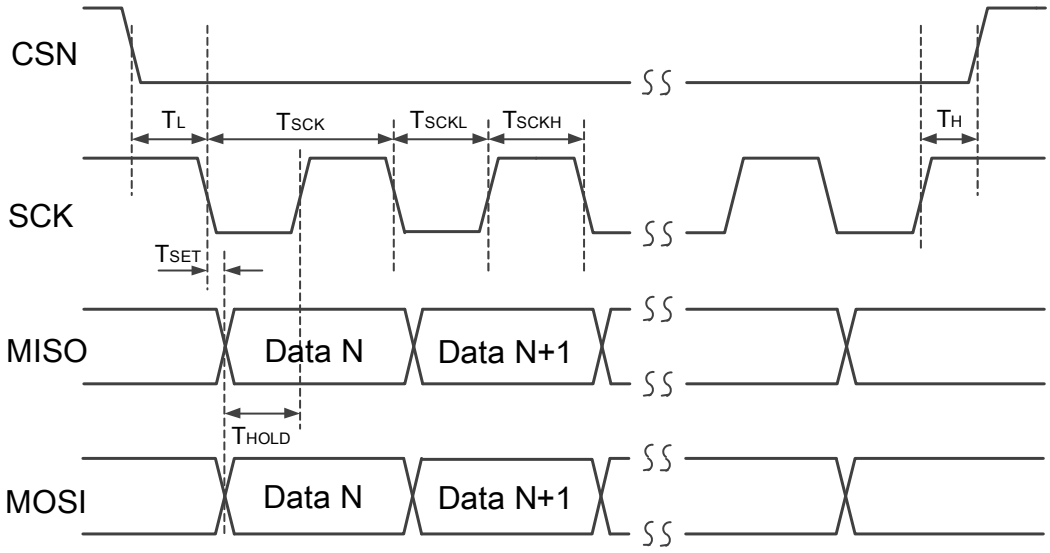


Figure 17: SPI Timing Diagram

Symbol	Notes	Min	Max.	Unit
T_L	Time between CSN falling edge and SCK falling edge	250		ns
T_{SCK}	Clock period	400 (1)		ns
T_{SCKL}	Low period of clock	200 (2)		ns
T_{SCKH}	High period of clock	200 (2)		ns
T_{SET}	Setup time for MISO/MOSI data	50		ns
T_{HOLD}	Hold time for MISO/MOSI data	50		ns
T_H	Time between SCK last rising edge and CSN rising edge	0.5•T_{SCK}		ns

Notes:

(1) The MT6813 has a burst mode. When this mode is enabled, the chip internal clock frequency is doubled and the minimum T_{SCK} also could be reduced to 200ns

(2) The MT6813 has a burst mode. When this mode is enabled, the chip internal clock frequency is doubled and the minimum T_{SCKL} and T_{SCKH} also could be reduced to 100ns

7.5.2.4-Wire SPI

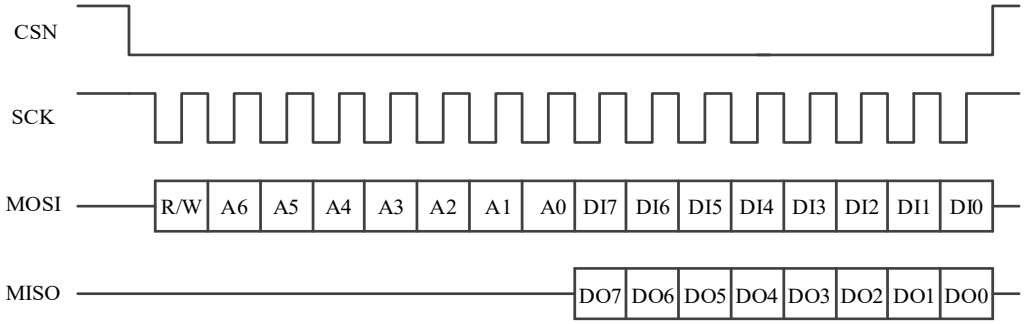


Figure 18: 4-Wire SPI Timing

An SPI data transfer starts with the falling edge of CSN and stops at the rising edge of CSN. SCK is the Serial Port Clock and it is controlled by the SPI master, it is high when there is no SPI transmission. MOSI (master input slave output) and MOSI (mast input slave output) is the Serial Port Data Input and Output, it is driven at the falling edge of CLK and should be captured at the rising edge of CLK.

Bit 0: R/W bit, when it is 0, the data D7~D0 is written into the device，when it is 1, the data D7~D0 from the device is read. In latter case, the chip will drive data at the start of bit 8.

Bit 1-7: Address A6~A0. This is the address field of the indexed register.

Bit 8-15: Data DI7~DI0 (write mode). This is the data that will be written into the device (MSB first).

Bit 8-15: Data DO7~DO0 (read mode). This is the data that will be read from the device (MSB first).

7.5.3. 3-Wire SPI

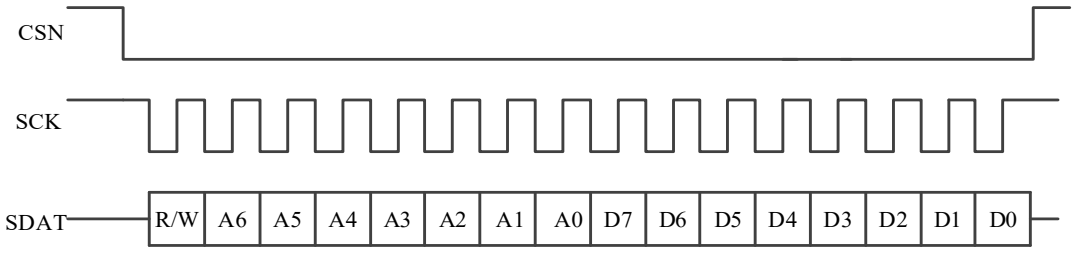


Figure 19: 3-Wire SPI Timing

An SPI data transfer starts with the falling edge of CSN and stops at the rising edge of CSN. SCK is the Serial Port Clock and it is controlled by the SPI master, it is high when there is no SPI transmission. SDAT is the Serial Port Data Input and Output, and it is driven at the falling edge of CLK and should be captured at the rising edge of SCK.

Bit 0: RW bit. When 0, the data D7~D0 is written into the device. When 1, the data D7~D0 from the device is read. In latter case, the chip will drive data at the start of bit 8.

Bit 1-7: address A6~A0. This is the address field of the indexed register.

Bit 8-15: data D7~D0 (write mode). This is the data that will be written into the device (MSB first).

Bit 8-15: data D7~D0 (read mode). This is the data that will be read from the device (MSB first).

7.5.4. SPI Read Angle Register (e.g. 4-Wire SPI)

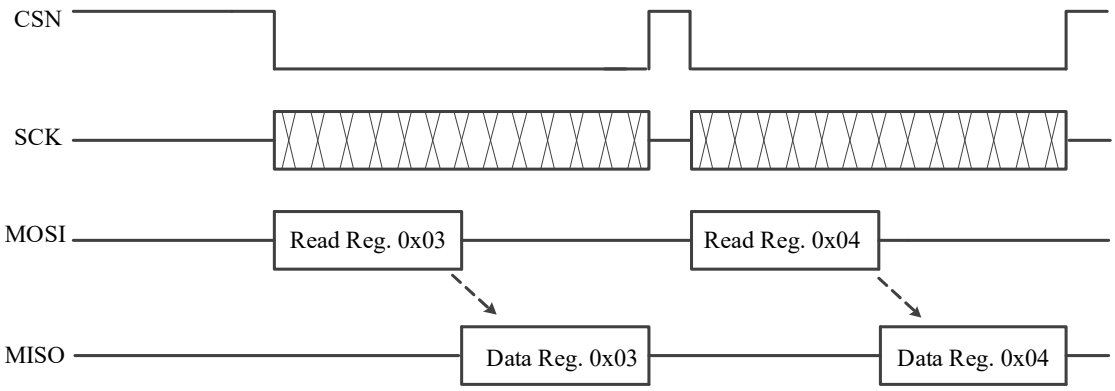


Figure 20: 4-Wire SPI Single Byte Read Angle Registers

Angle Data Register

Reg. Addr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0X03	Angle<13:6>							
0X04	Angle<5:0>						No_Mag_Warning	Parity Check

The 0~360° absolute angle θ could be calculated by the below formula:

$$\theta = \frac{\sum_{i=0}^{13} 2^{Angle<i>}}{8192} \bullet 360°$$

Parity Check

Bit 0x04[1] is a diagnosed bit for No Magnet Detected. When the MT6813 could not detect enough magnetic field for proper operation, this bit is set to high.

Bit 0x04[0] is a parity check bit for the data of 0x03[7:0] and 0x04[7:1]. When the 15 bits of 0x03[7:0] and 0x04[7:1] have an odd number of logic '1', 0x04[0]=1, otherwise 0x04[0]=0.

e.g. Under normal operation, get data 0x03=8F, 0x04=19, the parity check is correct
e.g. Under normal operation, get data 0x03=8F, 0x04=18, the parity check is wrong.

The MT6813 provides an SPI burst read mode for faster data rate than single byte read mode as shown in Figure 21.

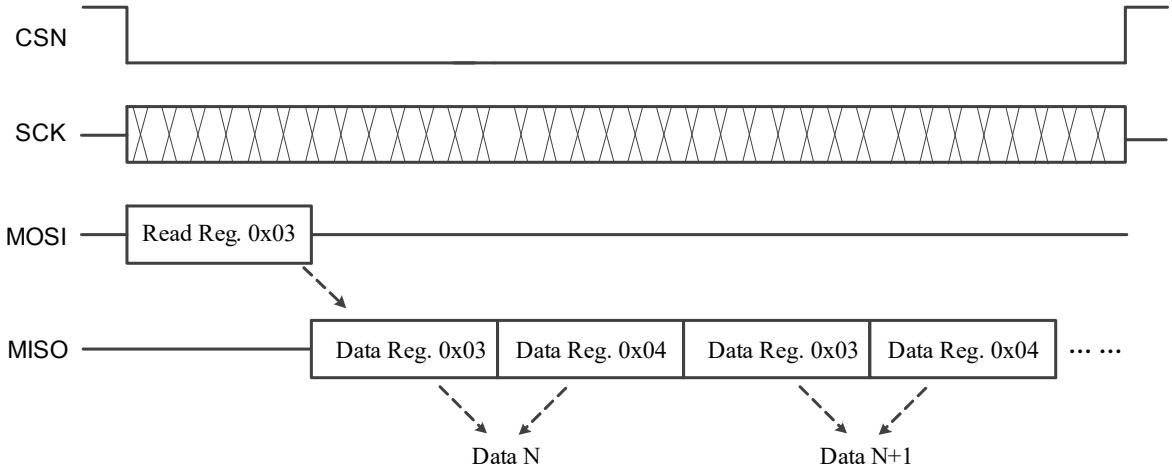


Figure 21: 4-Wire SPI Burst Read Angle Registers

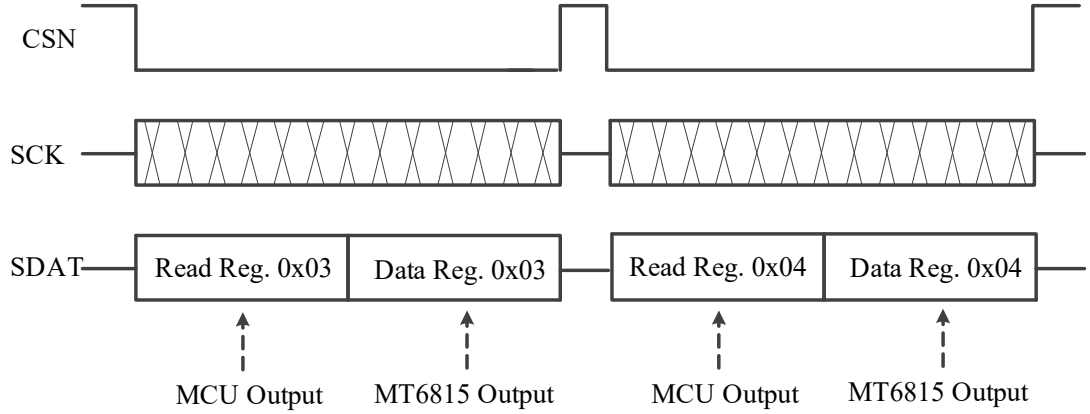


Figure 22: 3-Wire SPI Single Byte Read Angle Registers

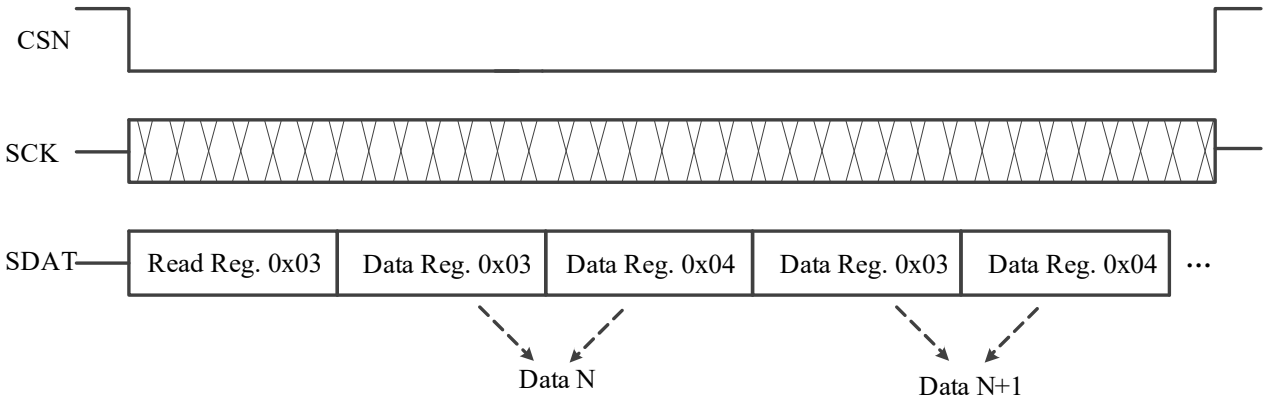


Figure 23: 3-Wire SPI Burst Read Angle Registers

8. Magnet Placement

The MT6813 is suitable for on-axis applications of angle measurement. The magnet should be mounted in a suitable environment where its magnetic field will not be distorted as shown in Figure 24.

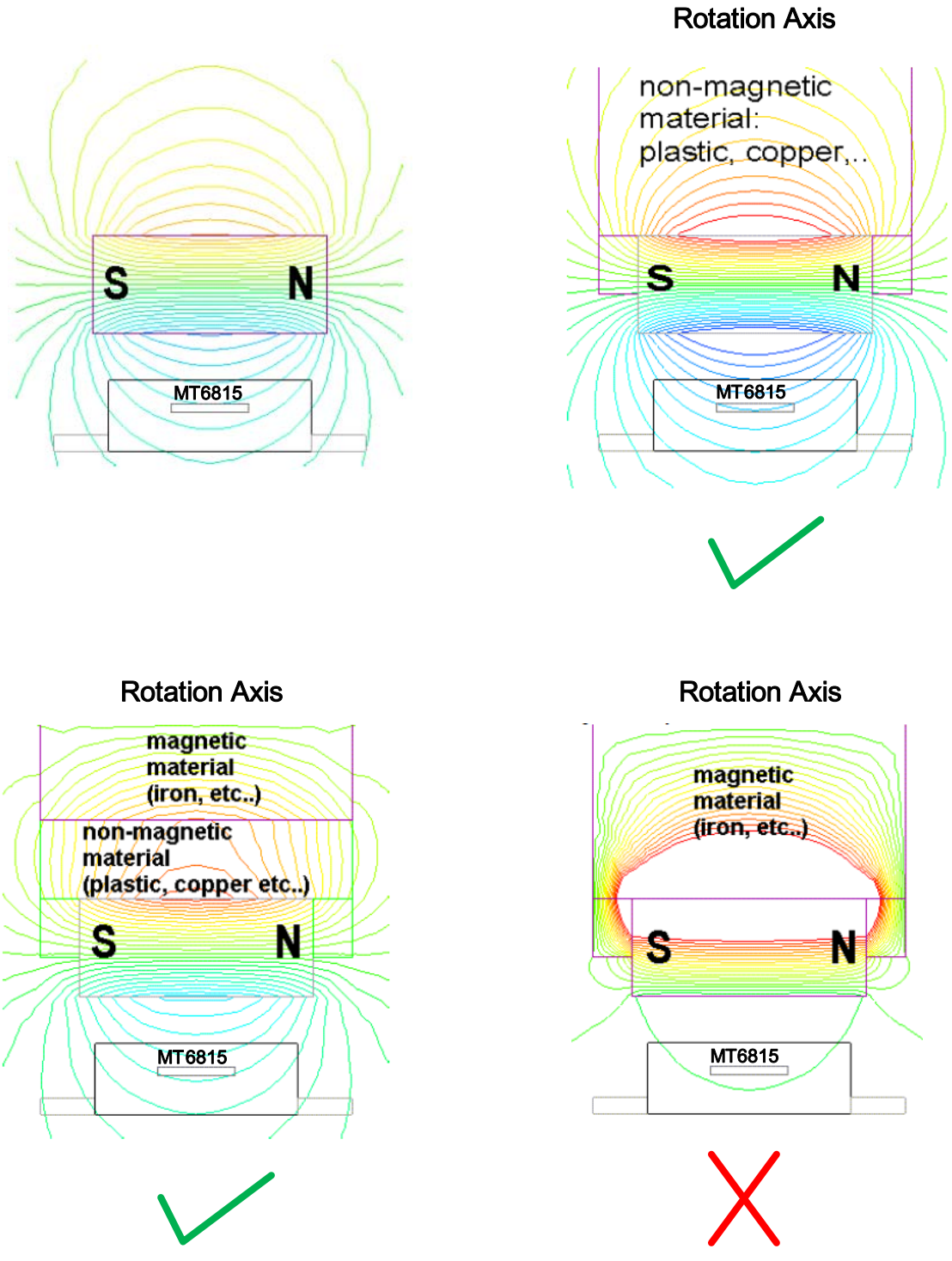
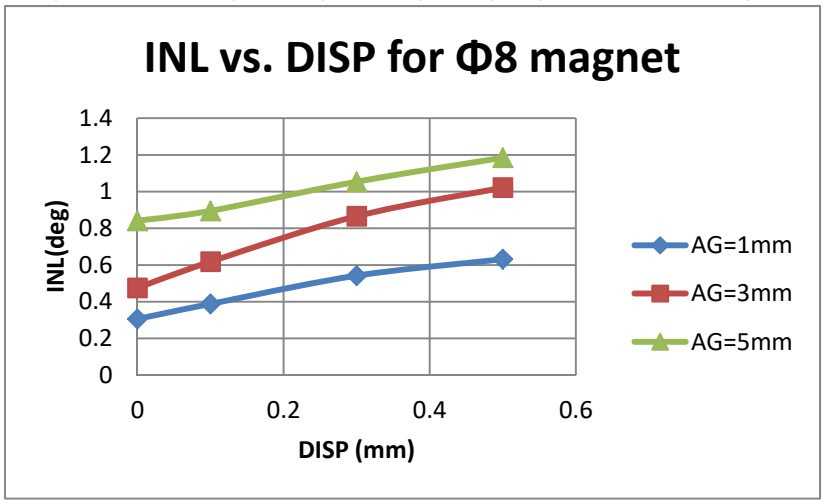
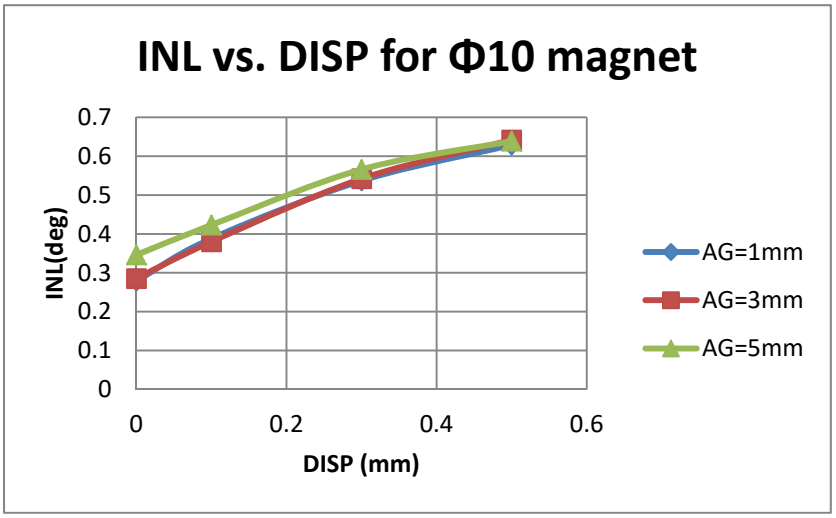
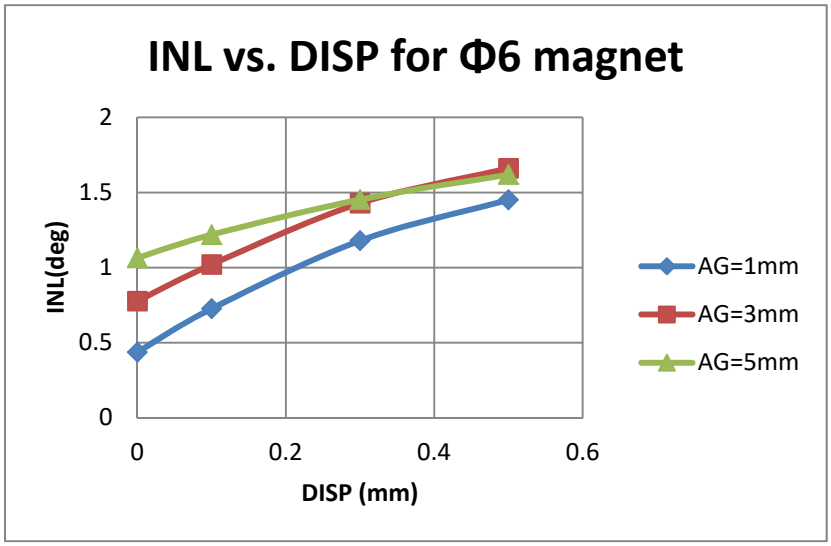


Figure 24: Magnet Mounted Reference

Also it is required that the magnet's center axis be aligned with the sensing element center of MT6815 with the air-gap as small as possible. Any misalignment introduces additional angle error and big air-gap also weakens the magnet field which could be sensed by the device. Magnets with larger radius are more tolerant to DISP (off-axis misalignment) and big AG (air-gap between Magnet and device).

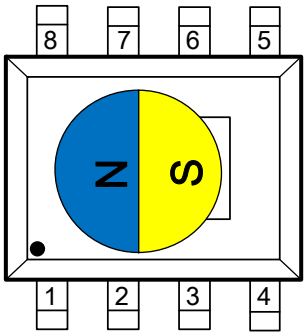




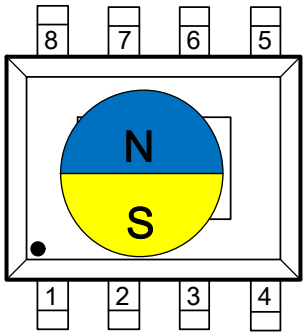


9. Mechanical Angle Direction

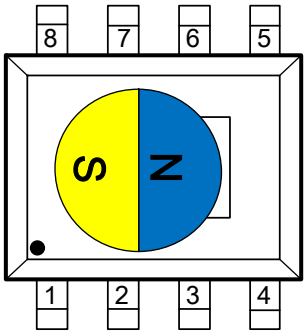
0 degree



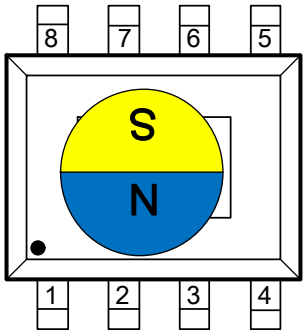
90 degree

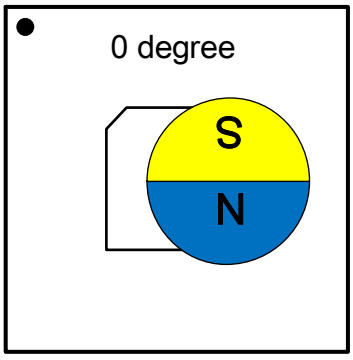


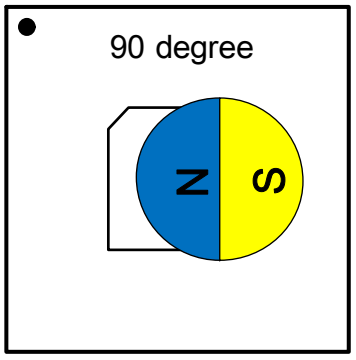
180 degree

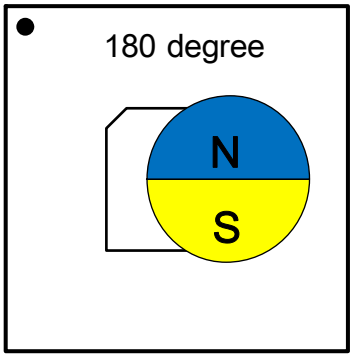


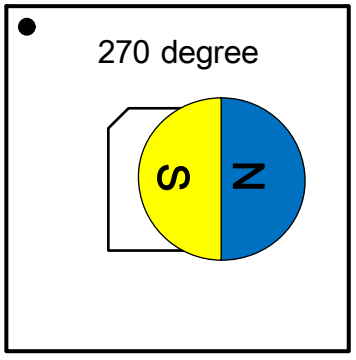
270 degree





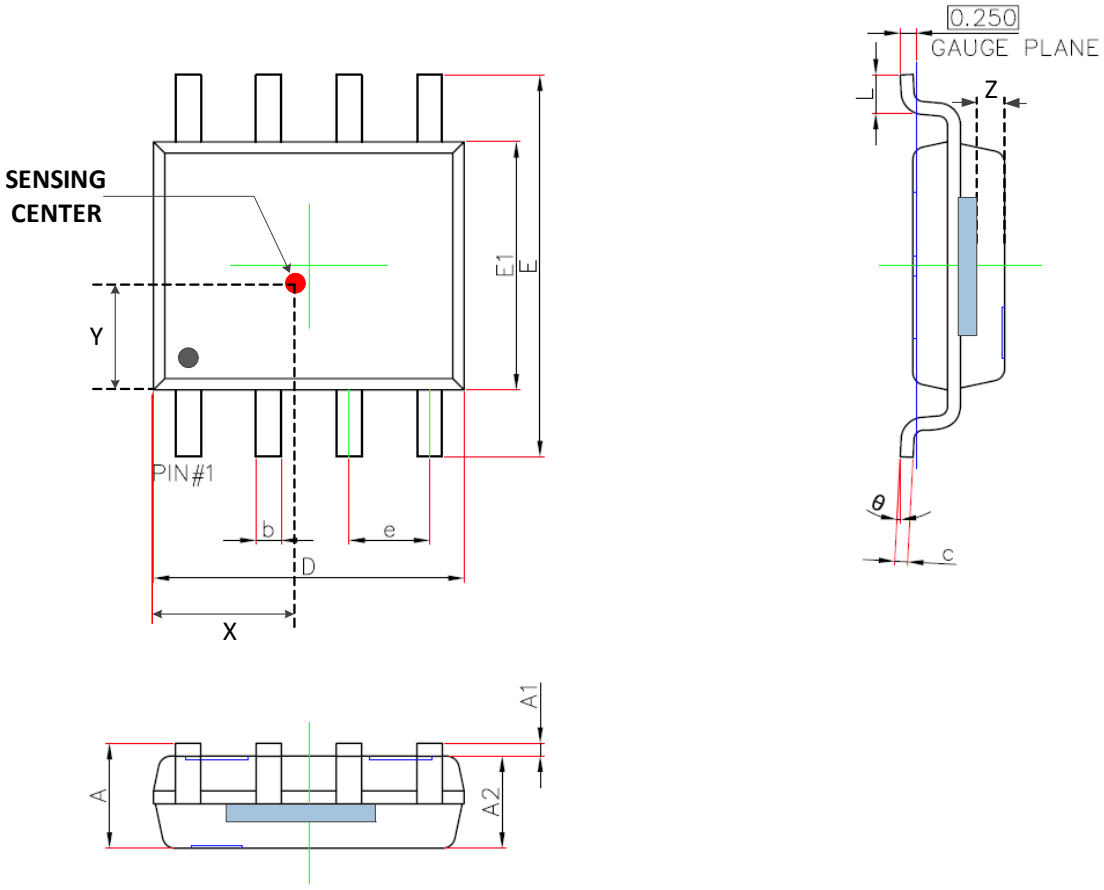






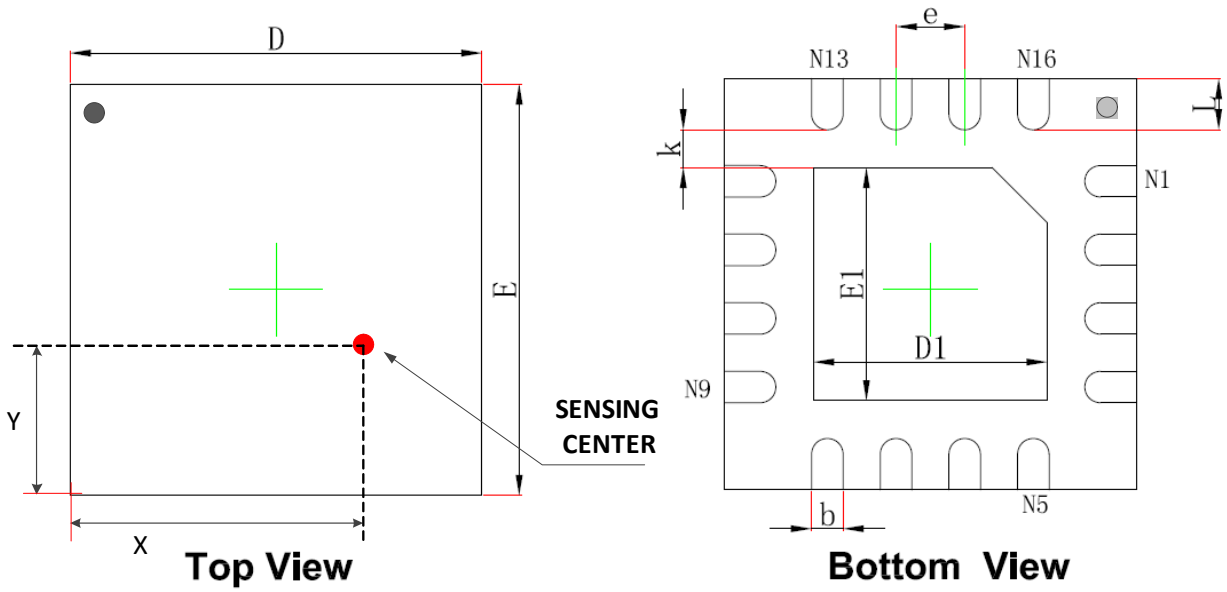
10. Package Designator

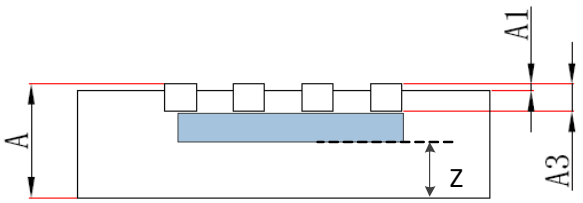
SOP-8



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
e	1.270(BSC)		0.050(BSC)	
L	0.400	0.800	0.016	0.031
θ	0˚	8˚	0˚	8˚
X	1.94	2.24	0.076	0.088
Y	1.71	2.01	0.067	0.079
Z	0.42	0.62	0.016	0.024

QFN-16





Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.203REF		0.008REF	
D	2.900	3.100	0.114	0.112
E	2.900	3.100	0.114	0.112
D1	1.600	1.800	0.063	0.071
E1	1.600	1.800	0.063	0.071
k	0.275REF		0.011REF	
b	0.180	0.300	0.007	0.012
e	0.500REF		0.020REF	
L	0.300	0.500	0.012	0.020
X	1.690	1.990	0.066	0.078
Y	1.110	1.410	0.043	0.055
Z	0.42	0.62	0.016	0.024